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Assessment of Potential Interactions between the Core Exit Thermocouple Signals and the Self-Powered Detector Signals in the AP1000™ In-core Instrumentation System

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M. D. Heibel*

Nuclear Services ES/PSDR Nuclear Operations

July 2010

Reviewer: J. G. Ewald*
Nuclear Power Plants DD/BSDI Electronic Systems Integration

Approved: G. F. Vincent*, Manager
Nuclear Services ES/PSDR Nuclear Operations

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Westinghouse Electric Company LLC
P.O. Box 355
Pittsburgh, PA 15230-0355

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1.0 INTRODUCTION

The AP1000™* In-core Instrumentation System (IIS) design contains hardware that places the Class 1E Core Exit Thermocouple (CET) signal wires used by the Class 1E Post-Accident Monitoring System (PAMS) and the Non-Class 1E Self Powered Detector (SPD) signal wires used by the On-line Power Distribution Monitoring System (OPDMS) into very close proximity with each other. The required separation distances identified in IEEE-384 (1981) between Safety and Non-Safety signals is not met in the Incore Instrument Thimble Assemblies (IITA) and the Mineral Insulated (MI) cable assembly hardware that route the CET and SPD signals from the Reactor Vessel Head (RVH) penetrations for the IITA to the Refueling Disconnect Panel (RDP) on the Containment Building Refueling Deck. Per the dictums in IEEE-384 (1981), since the minimum separation distance between the Safety and Non-Safety signals is not met, an analysis or testing of the potential interactions between the Safety and Non-Safety signals is required to demonstrate that credible faults in the Non-Safety signals will not cause loss of the Safety functions. This report describes how the AP1000 IIS design satisfies the requirements of IEEE-384 (1981) such that any credible single fault in the Non-Class 1E SPD signals will not reduce the number of valid Class 1E CET inputs to the PAMS below the required minimum number (i.e. – 3 operable CET per core quadrant).

Four of the AP1000 IITA contain Non-Class 1E CET sensors that provide input to the Non-Class 1E Diverse Actuation System (DAS). The signal paths associated with these four CET providing inputs to the DAS introduce another potential path for a Non-Class 1E system fault to impact the PAMS operability. This document also identifies the measures used in the AP1000 IIS design to ensure that no credible fault in the DAS will cause loss of PAMS operability via interactions in the four IITA containing Non-Class 1E CET.

2.0 ANALYSIS DESCRIPTION

The AP1000 IIS and the PAMS both use signals output from the IITA. The AP1000 IITA contain metal sheathed Class 1E grounded junction Type-K CET used by the PAMS and Non-Class 1E metal sheathed Vanadium SPD elements used by the OPDMS feature of the IIS. Inside the IITA the Class 1E CET elements and the SPD elements are electrically isolated from each other by placing the active portions of the elements inside individual steel outer sheaths that share a common ground. The IITA are connected to Class 1E design and post-accident environmentally qualified MI cables that are used to route the CET and SPD signals from the RVH to the RDP that also electrically isolate the SPD and CET signals using steel outer sheaths with a common ground. The presence of two commonly grounded metallic barriers within the IITA probe assembly and in the MI cables makes it incredible for an SPD emitter signal to short directly to the CET element signal leads. Figure 1 presents the layout of an AP1000 IITA.

* AP1000 is a trademark of Westinghouse Electric Company LLC.

The CET signals and SPD signals share common Class 1E design and post-accident environmentally qualified MI cables from the Quickloc flanges on the Reactor Vessel Head until a location just beyond the cable RDP is reached. The CET signals used by the PAMS are then split into two Divisions and routed to Class 1E Containment Penetrations via Class 1E design and post-accident environmentally qualified cables. The SPD signals are also split into two corresponding Trains at the CET Division split location and routed separately from the RDP area via MI cables that also meet the 1E design and post-accident environmental qualification requirements to the two SPS cabinets located inside the Containment Building. The analog SPD currents are digitized inside the SPS cabinets and conditioned for transmission out of the containment via fiber-optic cables. The 4 CET signals used by the DAS are routed to Non-Class 1E penetrations via long Class 1E design and post-accident environmentally qualified MI cables. The SPD signals are split between the SPS cabinets such that all of the SPD signals input to one cabinet are associated with one Division of PAMS CET signals. The IITA containing CET that provide inputs to the DAS are divided evenly between the two SPS cabinets. Figure 2 provides a schematic representation the CET and SPD signal routing.

Since the SPD signals are not used for any Reactor Protection System functions, and the SPD signals are not required for post-accident use, the original input power supply scheme for the SPS Cabinets had each cabinet being supplied with redundant sources of Non-Class 1E power. During the Preliminary SPS Cabinet Design Review, the issue of compliance with IEEE-384 (1981) requirements related to isolation of Class 1E and Non-Class 1E circuits within the IIS was discussed. Specific questions on the consequences of a potential unbounded power supply surge or over-voltage input to the SPS cabinets during LOCA or other harsh post-accident conditions on the operability of the PAMS CET signal inputs to the PAMS were raised.

Since the SPD signals have no direct Reactor Protection applications, the SPS cabinets are not specifically designed to operate in a post-accident environment. If it is assumed that none of the Non-Class 1E qualified and non-post accident environment qualified over-voltage or surge protection contained in the SPS cabinet electronics operates as designed (due perhaps to harsh environmental conditions in containment in the post-accident environment), and an over-voltage or surge voltage from the electrical power source providing input to the SPS cabinets is able to propagate backwards to the SPD input signals through the SPS circuitry without attenuation or shorting to ground, it is considered credible that a sufficiently large over-voltage or a voltage surge at the SPS cabinet power supply inputs could cause at least a momentary loss of all Class 1E CET signals associated with the affected SPS cabinet via shorting between the SPD and CET wires in the backshell of the IITA or MI cable electrical connectors. If the over-voltage or transient surge condition were to occur on both SPS cabinets, then the result could be that all of the CET signals needed by the PAMS become inoperable. Reference 2 provides the IIS design configuration established to prevent these potentially adverse consequences. Details of the analysis performed to evaluate the design relative to the requirements of IEEE-384 (1981) are provided below.

Reference 1 provides the historic maximum over-voltage value that was identified to be credible on low voltage circuits in Westinghouse Nuclear Power Plant designs that run cable per nuclear industry standards. [

]^{a,c} The USNRC SER contained in Reference 1 indicates regulatory acceptance of the identified maximum credible voltage values. The Design Requirements for the MI Cable and IITA electrical connector hardware identified in Reference 2 require that manufacturing or proof testing be performed to demonstrate compliance with a [ ]^{a,c} peak voltage CET functional interaction exclusion requirements. This hardware testing requirement satisfies the requirements for testing or analysis of Associated Circuit interactions with Class 1E circuits contained in IEEE-384 (1981) for over-voltage conditions.

In order to further mitigate the possibility of a transient surge voltage condition in the SPS cabinet's input power supply in excess of [ ]^{a,c} disabling both Divisions of the CET signals used by the PAMS, the AP1000 IIS design identified in Reference 2 supplies different Divisions of Safety Power to the IIS SPS cabinets with the power cables routed in separate shielded conduits to the SPS cabinets. Assigning each SPS cabinet and its corresponding PAMS Division to a different Class 1E power bus ensures that any fault on the SPS cabinets input power supplies will only occur on one SPS cabinet and can therefore only disable one Division of the CET signals used by PAMS. Since the PAMS is still operable with only one operable Division of CET signals, the potential for a loss of the minimum required PAMS functionality due to any single SPS cabinet input power issue is not credible. Figure 3 illustrates the power supply scheme to the SPS cabinets to be used that is consistent with the configuration of Associated Circuit item 2 in Figure 1 of IEEE 384 (1981).

Additionally, four of the 42 AP1000 IITA contain CET that produce signals which are routed to the DAS. The DAS is a Non-Class 1E system. These signals represent another potential path for surge or over-voltage faults to enter the IIS from the DAS that could affect PAMS CET signal availability. As identified in Reference 2, an analysis of the maximum credible surge voltage output from DAS to the DAS CET signal leads that could produce an interaction with IIS concludes the peak credible surge voltage generated by the DAS per USNRC Reg. Guide 1.180 Rev. 1 is the same as the IIS IITA and CET cable and electrical connector hardware voltage environmental and electromagnetic interference qualification limit requirements contained in Tier 2, Appendix Section 3D.4.1.2 of Revision 17 of the AP1000 Design Control Document (DCD). The DCD hardware requirements specifically require that the IIS IITA and associated cables be qualified to meet Reg. Guide 1.180 peak surge voltage pulse levels. This result ensures that if there is a voltage surge from DAS that propagates down through the DAS CET signal leads to the associated SPD cables, there will be no credible, systematic shorting of DAS CET signals to the associated SPD signal leads. Therefore there is no credible mechanism to cause loss of the minimum required amount PAMS CET coverage.

Reference 2 identifies the analysis performed for the IIS for a nominal, un-faulted input power supply condition needed to address IEEE 384 (1981) Section 5.6 item 4 which states that Non-Class 1E circuits "are not required to be physically separated or electrically isolated from associated circuits provided that . . . the Non-Class 1E circuits are analyzed to demonstrate that Class 1E circuits are not degraded below an acceptable level." The analysis that supports the Non-Class 1E Circuit analysis required by IEEE 384 (1981) for the IIS with a nominal input power supply condition called out in Reference 2 includes the IITA and MI cable and connector design requirement that the integrity of the IITA and MI cable and connectors are fully demonstrated at or above the maximum surge or over-voltage that could be generated in the IIS with nominal external power supply conditions and also addresses the following:

1) Ensure that no fault originating within the SPS cabinets can result in fault voltages at the reactor vessel head or refueling disconnect panel connectors of greater than [ ]^{a,c} between the connector pins.
2) Ensure that inadvertent disconnection or failures of any IITA emitter wire or wires either at the SPS cabinet, or anywhere in the cabling between the IITA and the SPS cabinet will not cause voltage charge-up on the SPD emitter wire exceeding [ ]^{a,c} during normal plant operation, thus preventing the fault voltage from affecting the associated CET.

The analysis identified in Reference 2 concludes that there is no credible fault originating in the IIS SPS cabinets or cables with nominal input electrical power that could credibly cause the loss of the CET required for PAMS operability. Figure 3 provides a schematic representation of the 1E/Non-1E boundaries contained within the AP1000 IIS.

3.0 ANALYSIS CONCLUSION

The results of the analysis documented in Reference 2, coupled with the use of safety power supply sources that have the maximum credible over-voltage values of [ ]^{a,c} documented in Reference 1, and the use of different Divisions of Safety Power and the DAS CET interaction potential analysis captured through Reference 2, ensures that the Non-Class 1E Circuits in the IIS will not interfere with the safety functions of the Class 1E CET under any credible operating conditions. These analysis results demonstrate that the consequences of any credible electrical fault associated with the AP1000 IIS hardware will not cause the loss of the required CET inputs to the PAMS.

4.0 REFERENCES

1. WCAP-8892, Rev. 2, "Westinghouse 7300 Series Process Control System Noise Test," Westinghouse Electric Corporation, 1977.
2. APP-GW-GEE-1121, Rev. 0, "External Power Supply Requirements for AP1000 Incore Instrumentation System (IIS) Signal Processing System (SPS) Cabinets," Westinghouse Electric Company LLC.

a,c

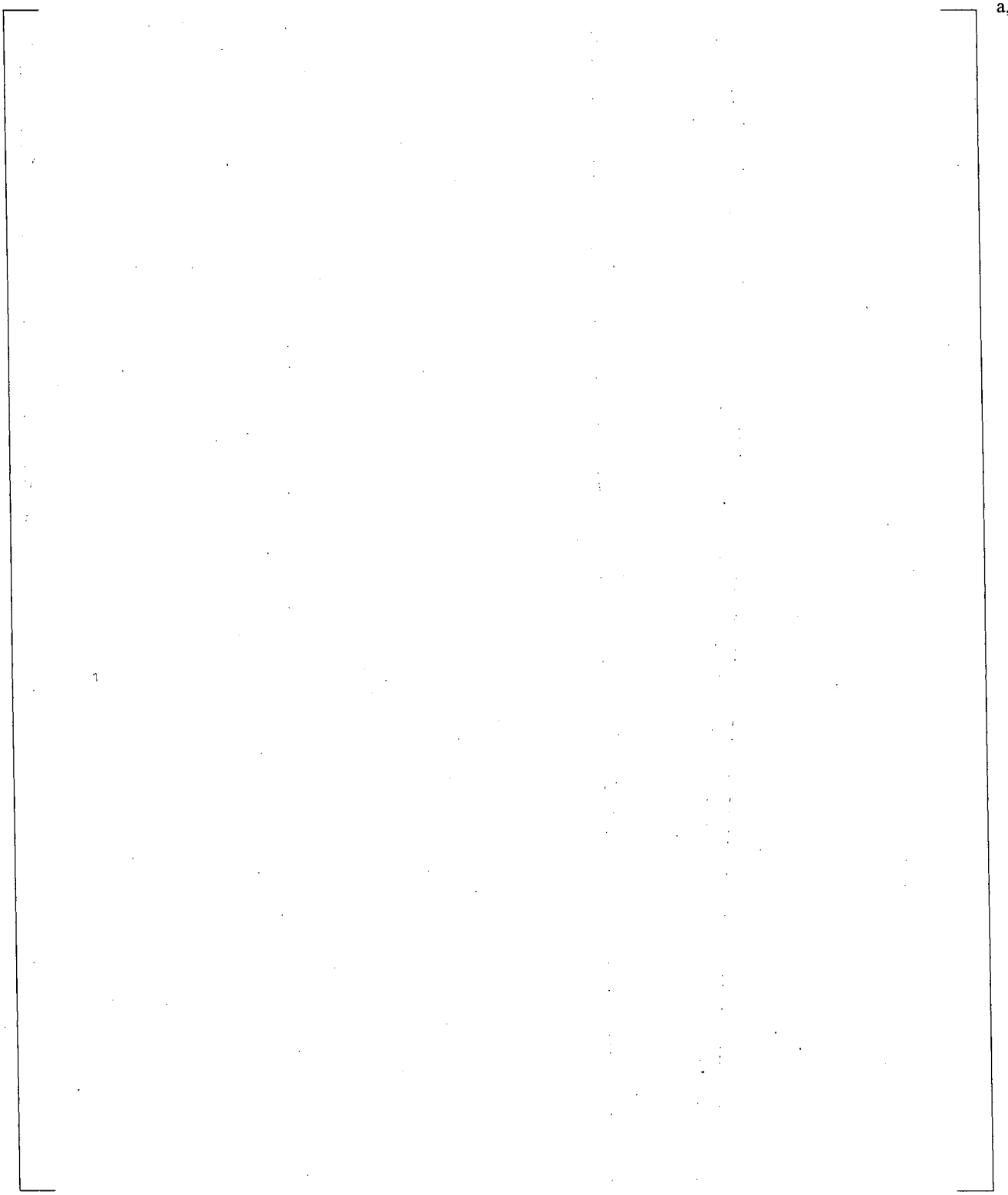

Figure 1 – IITA Layout Drawing

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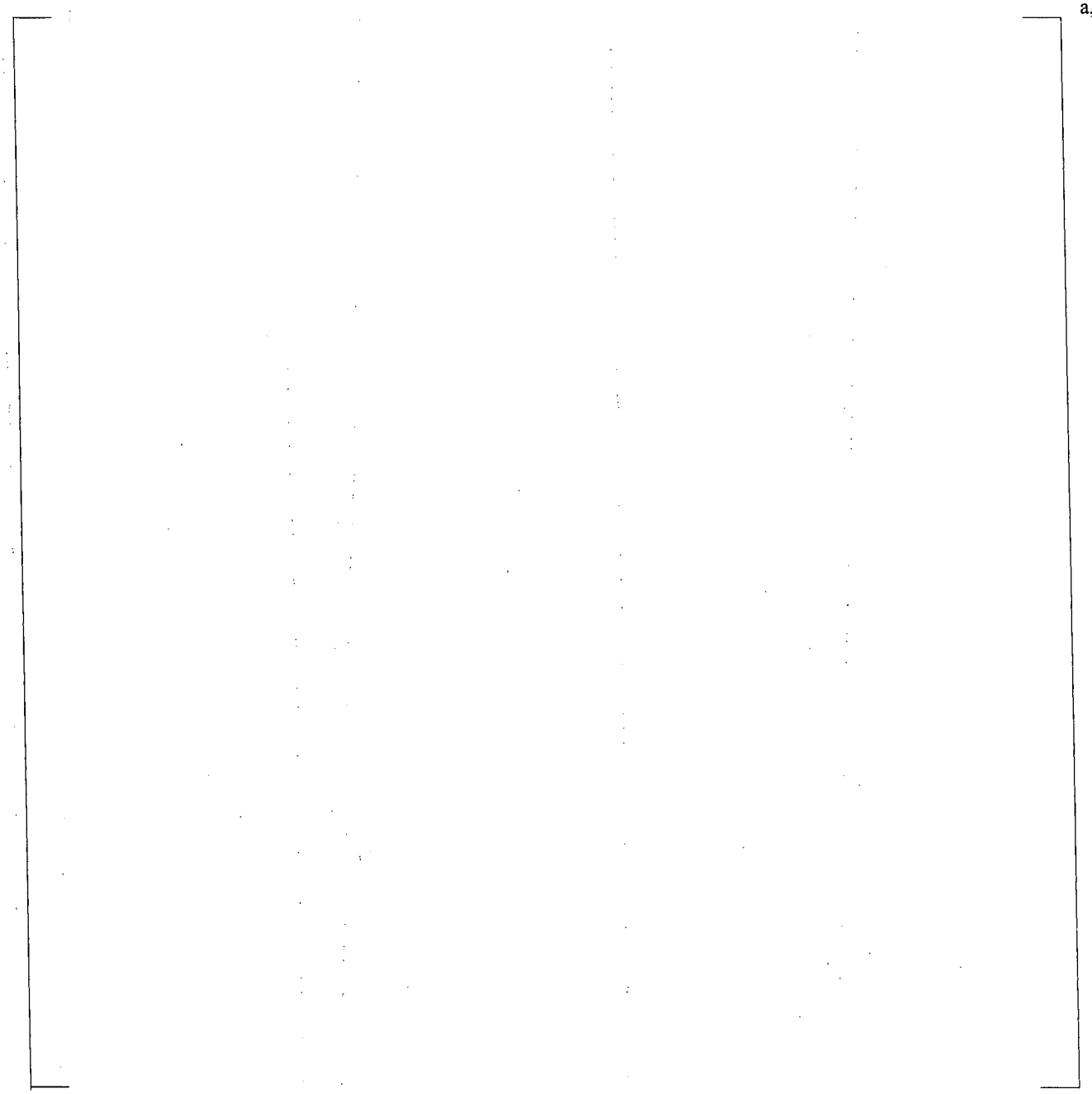

Figure 2 – AP1000 IIS Sensor Configuration Schematic

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Figure 3 – AP1000 IIS IITA and SPS Cabinet Interface Schematic